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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/961,229	09/20/2001	Vladimir Rumennik	003692P007XD4	4375

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EXAMINER
HU, SHOUXIANG

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/961,229	Applicant(s) RUMENNIK ET AL.
	Examiner Shouxiang Hu	Art Unit 2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *50-57 and 93-111* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *50-57 and 93-111* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. This application is a divisional one of U.S. Serial No. 09/574,563, filed on 5/17/2000, which itself is a divisional one of 09/245,030, filed on 2/5/99, now U.S. Patent 6,207,994, which in turn is a continuation-in-part of U.S. Serial No. 08/744,182, filed on 11/5/96.

Pending Claims

2. Claims 50-57 and 93-111 are pending and remain active in this application, in view of the 9/20/2001 amendment.

Claim Objections

3. Claims 93-111 are objected to because of the following informalities and/or defects:

In claims 93 and 103 (line 3), the term of "a epitaxial" should read as: --an epitaxial--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 93-102 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 93 recites the limitation of "a buried layer of the first conductivity type disposed within the portion of the epitaxial layer spaced-apart from the drain diffusion region", but it fails to clarify whether it is the portion of the epitaxial layer, or it is the buried layer, that is spaced-apart from the drain diffusion region.

Appropriate correction is required.

Double Patenting

5. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefore..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claims 50 –57 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-7 of prior U.S. Patent No. 6,207,994. This is a double patenting rejection.

The term of "at least one buried layer" recited in Claim 50 of the instant invention can be interpreted as meaning either "one buried layer" or "plurality of buried layers".

Accordingly, when it is interpreted as meaning "plurality of buried layers", the claimed invention of an HVFET as defined in Claims 50-57 of the instant invention is a same invention as the one defined in Claims 1-7 of U.S. Patent No. 6,207,994.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

7. Claims 93-95 and 99-102, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being obvious over Williams et al. ("Williams"; 5,386,136; of record) in view of Yamanishi et al. ("Yamanishi"; JP404107877A; of record), or, in the alternative, as being obvious over Yamanishi in view of Williams.

Williams discloses an HVFET (Fig. 4), comprising: a p-type substrate (205); an n-type epitaxial layer (206); a p-type diffusion region or first region (203 and a portion of 204), which inherently forms a junction with the surrounding n-type epitaxial layer (206); an n-type source diffusion region (202) with a source electrode (220); an isolated gate (209) above an IGFET channel region; an n-type drain region (207) with a drain electrode (208); an additional p-type buried region (201); and an additional p-type diffusion region or second region (the upper portion of 204).

Williams does not expressly disclose that the HVFET can further include a p-type buried region in the n-type epitaxial layer between the channel and the drain. However,

one of ordinary skill in the art would readily recognize that the n-type epitaxial layer between channel and the drain in Williams inherently functions as an extended drain region therein. And, Yamanishi teaches to form an HVFET (see Fig. 1) with a p-type buried region (10) in an n-type extended drain region between (and separated from the) channel and the drain for increasing the breakdown voltage and reducing the on-state resistance. It is noted that the p-type buried layer (10) can inherently form two JFET-type conduction channels above and below it in the in the first region.

Therefore, it would have been obvious to one of ordinary skilled in the art at the time the invention was made to incorporate the p-type-buried region of Yamanishi into the HVFET of Williams, so that an HVFET with high breakdown voltage and low on-state resistance would be achieved.

Or, in the alternative, Yamanishi discloses the claimed invention (see Fig. 1 and the English abstract) except that Yamanishi does not explicitly disclose in English what are the conductivity types for the individual regions, such as p-type for the substrate (15), and that the extended drain region can be formed of an epitaxial layer. However, as evidenced in Williams (as discussed above), one of ordinary skill would readily recognize what the proper conductivity types should be for these individual regions in order to achieve commonly recognized FET functionality, and that the extended drain region can be formed of an epitaxial layer for better doping control (concentration accuracy and uniformity).

Therefore, it would also have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the individual regions of proper

conductivity types and the n-type epitaxial layer of Williams into the HVFET of Yamanishi, so that an HVFET with commonly recognized FET functionality and with better doping control in the extended drain region would be achieved.

Regarding claim 94, the buried layer in Yamanishi is spaced-apart from any junction.

Regarding claims 99 and 108, although Williams does not disclose that the buried region is connected to the substrate, Yamanishi further teaches that the buried p-type layer (10) can be biased reversely to the drain area (see the English Abstract). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the HVFET, collectively taught by Williams and Yamanishi above, with the buried region being connected to the substrate, so that the desirable reverse bias between the p-type buried region and the drain area would be obtained, per the further teaching of Yamanishi.

Regarding claim 111, one of ordinary skill in the art would readily recognize that field plate members can be desirably included in the source/drain electrode for further improving the breakdown voltage, as further evidenced in Yamanishi (see the expanded S/D electrodes (6 and 5 in Fig. 1).

8. Claims 96-98 are rejected under 35 U.S.C. 103(a) as being obvious over Williams in view of Yamanishi, or, in the alternative, as being obvious over Yamanishi in

view of Williams, as applied to claims 93-95 and 99-111 above, and further in view of Colak (US 4,626,879).

The disclosures of Williams and Yamanishi are discussed as applied to claims 93-95 and 99-111 above.

Although Williams and Yamanishi do not expressly disclose that the p-type buried layer can overlap the gate and/or extend beneath the drain region, Colak teaches to form an HVFET (Fig. 1) having a p-type buried layer (16) overlapping the gate (30) and extending beneath the drain region (24), for improving the punchthrough and avalanche breakdown characteristics (see the abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the above HVFET collectively taught by Williams and Yamanishi with the buried region overlapping the gate and extending beneath the drain region, as taught in Colak, so that an HVFET with improved punchthrough and avalanche breakdown characteristics would be obtained.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is (703) 306-5729. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers

for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

SH
April 14, 2003

Shouxiang Hu
Patent Examiner
TC2800